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EXAMINER	
WILLIAMS, LAWRENCE B	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

pair@tuchmanlaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/614,523	FURRER ET AL.	
	Examiner	Art Unit	
	LAWRENCE B. WILLIAMS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22 and 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22, 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

2. Applicant's arguments, see Applicant Arguments/Remarks Made in an Amendment filed 02/09/2010, with respect to the rejection(s) of claim(s) 1-9, 16-22, 28, 10-15 under 35 U.S.C.102(b) and 35 U.S.C. 103(a), respectively have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Takeda (US Patent 5,734,808) and Fu (US Patent 6,457,087 B1).

Claim Objections

3. Claims 1-3 are objected to because of the following informalities: The examiner suggests, "A communication device" in the preamble. Appropriate correction is required.

4. Claims 20-22 are objected to because of the following informalities: The examiner suggests, "A transceiver unit" in the preamble. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 2-3, 17-18, 21, 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Takeda (US Patent 5,734,808).

(1) Regarding claim 2, Takeda discloses in Fig. 1, a communication device for processing an outgoing packet, the device comprising: a plurality of signal processing units (pipeline processing register, data processing) connected in sequence, each signal processing unit being clocked by a common clock signal (BCLK); and a control line (Pipeline Control) to which each signal processing unit is connected, the control line communicating flow control information to stall at least one of the preceding signal processing units for feedback control of the signal processing units (col. 2, lines 55-60; Takeda discloses the pipeline control means permitting data transfer only when there is processing data in a pipeline register in a previous stage. Thus a stall or equivalent would be inherently be implemented in a preceding signal processing unit).

(2) Regarding claim 3, Takeda discloses in Fig. 1, a communication device for processing an incoming packet, the device comprising: a plurality of signal processing units (pipeline register, data processing) connected in sequence thereby forming a signal processing chain, each signal processing unit being clocked by a common clock signal (BCLK); and a control line (pipeline control) to which each signal processing unit is connected, the control line communicating flow control information to stall at least one of the signal processing units following in the signal processing chain for feedforward control of the signal processing units (col. 2, lines 55-60; Takeda discloses permitting data transfer only when there is processing data

in a pipeline register in a previous stage. Thus if no processing data in a pipeline register in a previous stage, a stall or equivalent would be inherent to following signal processing units).

(3) Regarding claim 11, Takeda also discloses in Fig. 3, the device according to claim 2, wherein each signal processing unit is connected via a logic unit to the control line (col. 7, lines 51-65; Takeda discloses the configuration of the pipeline control sections).

Thus it would have been obvious to one of ordinary skill in the art to implement the method as taught by Takeda et al. as a method of implementing data driven pipeline processing.

(4) Regarding claim 12, Takeda also discloses in Fig. 3, the device according to claim 3, wherein each signal processing unit is connected via a logic unit to the control line (col. 7, lines 51-65; Takeda discloses the configuration of the pipeline control sections).

Thus it would have been obvious to one of ordinary skill in the art to implement the method as taught by Takeda et al. as a method of implementing data driven pipeline processing.

(5) Regarding claim 14, Takeda also discloses in Fig. 3, the device according to claim 11, wherein the logic unit comprises an OR gate (col. 7, lines 51-65; Takeda discloses the configuration of the pipeline control section comprising OR gate, element 554).

(6) Regarding claim 15, Takeda also discloses in Fig. 3, the device according to claim 12, wherein the logic unit comprises an OR gate (col. 7, lines 51-65; Takeda discloses the configuration of the pipeline control section comprising OR gate, element 554).

(7) Regarding claim 17, Takeda also discloses wherein the flow control information comprises a hold information indicating to the signal processing unit receiving the hold information to stop processing (col. 2, lines 55-60).

(8) Regarding claim 18, Takeda also discloses wherein the flow control information comprises a hold information indicating to the signal processing unit receiving the hold information to stop processing (col. 2, lines 55-60).

(9) Regarding claim 21, Takeda discloses a transceiver unit adapted to communicate with a buffer unit via a bus system, the transceiver unit comprising, a transceiver controller (Fig. 15A, Out Put control, 220 controls transceiver of Fig. 1. Transceiver in the sense of receiving data and transmitting processed data) and a communication device (pipeline processing device of Fig. 1), both transceiver controller and communication device being interconnected, said communication device including a plurality of signal processing units (pipeline processing register, data processing) connected in sequence, each signal processing unit being clocked by a common clock signal (BCLK); and a control line (Pipeline Control) to which each signal processing unit is connected, the control line communicating flow control information to stall at least one of the preceding signal processing units for feedback control of the signal processing units (col. 2, lines 55-60; Takeda discloses the pipeline control means permitting data transfer only when there is processing data in a pipeline register in a previous stage. Thus a stall or equivalent would be inherently be implemented in a preceding signal processing unit).

(10) Regarding claim 22, Takeda a transceiver unit adapted to communicate with a buffer unit via a bus system, the transceiver unit comprising, a transceiver controller (Fig. 15A, Out Put control, 220 controls transceiver of Fig. 1. Transceiver in the sense of receiving data and transmitting processed data) and a communication device (pipeline processing device of Fig. 1), both transceiver controller and communication device being interconnected, said communication device including a plurality of signal processing units (pipeline processing register, data

processing) connected in sequence, each signal processing unit being clocked by a common clock signal (BCLK); and a control line (Pipeline Control) to which each signal processing unit is connected, the control line communicating flow control information to stall at least one of the signal processing units following in the signal processing chain for feedforward control of the signal processing units (col. 2, lines 55-60; Takeda discloses permitting data transfer only when there is processing data in a pipeline register in a previous stage. Thus if no processing data in a pipeline register in a previous stage, a stall or equivalent would be inherent to following signal processing units).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 4, 10, 13, 16, 19, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fu (US Patent 6,457,087 B1) in view of Takeda (US Patent 5,734,808).

(1) Regarding claim 1, Fu discloses in Fig. 9, a communication device for processing outgoing and incoming packets, the device comprising: a plurality of signal processing units (CIU, 208; BBU, 206) connected in sequence, each signal processing unit being clocked by a common clock signal (col. 12, lines 36-40; Fu discloses a clock signal transmitted along with the data to insure proper reception at the receiving device); a mode line connected to each signal processing unit for switching each signal processing unit between a transmit mode and a receive

mode (control signals 282; col. 13, line 61- col. 14, line 5); and a control line to which each signal processing unit is connected, the control line communicating flow control information (flow control line, 284) either in the transmit mode to at least one of the preceding signal processing units or in the receive mode to at least one of the following signal processing units (flow control line 284; Fu does not explictly use the language of communicating flow control information either in the transmit mode to at least one of the preceding processing units or in the receive mode to at least one of the following signal processing units. Lee et al. does teach the FCU controls the flow of data between the devices and includes transactions that acknowledge and interrupt and in Fig. 9 discloses the flow control signal as bi-directional which would imply communicating flow control information either in the transmit mode to at least one of the preceding signal processing units or in the receive mode to at least one of the following signal processing units).

However, the examiner points to Takeda et al. who teaches that it is well known in the art to use a flow control line to communicate flow control information in a transmit mode to one of preceding signal processing units. Takeda teaches a pipeline processing device wherein he teaches sequential transfer of data and communicating flow control information in a transmit mode to at least one of the preceding signal processing units (col. 2, lines 55-60; col. 3, lines 50-64; Takeda et al. teaches processing data transferred only when there is processing data in the previous stage).

Thus it would have been obvious to one of ordinary skill in the art to implement the method as taught by Takeda et al. as a method of implementing data driven pipeline processing.

(2) Regarding claim 4, Fu also discloses wherein each signal processing unit comprises a multiplexing unit. Fu discloses the control signals 282 in either mode are time multiplexed into four control bits per packet (col. 13, line 61- col. 14, line 5) inherently implying a multiplexer in the signal processing units.

(3) Regarding claim 10, Takeda also discloses in Fig. 3, wherein each signal processing unit is connected via a logic unit to the control line (col. 7, lines 51-65; Takeda discloses the configuration of the pipeline control sections).

Thus it would have been obvious to one of ordinary skill in the art to implement the method as taught by Takeda et al. as a method of implementing data driven pipeline processing.

(4) Regarding claim 13, Takeda also discloses in Fig. 3, wherein the logic unit comprises an OR gate (col. 7, lines 51-65; Takeda discloses the configuration of the pipeline control section comprising OR gate, element 554).

Thus it would have been obvious to one of ordinary skill in the art to implement the method as taught by Takeda et al. as a method of implementing data driven pipeline processing.

(5) Regarding claim 16, Takeda also discloses wherein the flow control information comprises a hold information indicating to the signal processing unit receiving the hold information to stop processing (col. 2, lines 55-60).

Thus it would have been obvious to one of ordinary skill in the art to implement the method as taught by Takeda et al. as a method of implementing data driven pipeline processing.

(6) Regarding claim 19, Fu also discloses wherein each signal processing unit is usable for the transmit and receive mode (Fig. 9 discloses the signal processing units bi-directional).

(7) Regarding claim 28, Fu discloses in Fig. 9, a baseband system comprising a communication device including a plurality of signal processing units (CIU, 208; BBU, 206) connected in sequence, each signal processing unit being clocked by a common clock signal (col. 12, lines 36-40; Fu discloses a clock signal transmitted along with the data to insure proper reception at the receiving device); a mode line connected to each signal processing unit for switching each signal processing unit between a transmit mode and a receive mode (control signals 282; col. 13, line 61- col. 14, line 5); and a control line to which each signal processing unit is connected, the control line communicating flow control information (flow control line, 284) either in the transmit mode to at least one of the preceding signal processing units or in the receive mode to at least one of the following signal processing units (flow control line 284; Fu does not explictly use the language of communicating flow control information either in the transmit mode to at least one of the preceding processing units or in the receive mode to at least one of the following signal processing units. Lee et al. does teach the FCU controls the flow of data between the devices and includes transactions that acknowledge and interrupt and in Fig. 9 discloses the flow control signal as bi-directional which would imply communicating flow control information either in the transmit mode to at least one of the preceding signal processing units or in the receive mode to at least one of the following signal processing units).

However, the examiner points to Takeda et al. who teaches that it is well known in the art to use a flow control line to communicate flow control information in a transmit mode to one of preceding signal processing units. Takeda teaches a pipeline processing device wherein he teaches sequential transfer of data and communicating flow control information in a transmit mode to at least one of the preceding signal processing units (col. 2, lines 55-60; col. 3, lines 50-

64; Takeda et al. teaches processing data transferred only when there is processing data in the previous stage).

Thus it would have been obvious to one of ordinary skill in the art to implement the method as taught by Takeda et al. as a method of implementing data driven pipeline processing.

9. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda (US Patent 5,734,808) as applied to claims 2, 3, respectively, in view of Sambamurthy et al. (US Patent 6,108,713).

Regarding claims 5 and 6, as noted above, Takeda discloses all limitations of claims 2 and 3. Takeda does not explictly disclose wherein each signal processing unit comprises a multiplexing unit. However, the signal-processing unit comprising a multiplexing unit is a minor detail. Sambamurthy et al. discloses in Fig. 4E, a signal processing unit (206) comprising a multiplexing unit (261).

It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Sambamurthy et al. as a method of permitting the simultaneous transmission of two or more trains of data.

10. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fu (US Patent 6,457,087 B1) in view of Takeda (US Patent 5,734,808) as applied to claim 1 above, and further in view of Koseki et al. (US Patent 4,686,668).

As noted above, the combination of Fu and Takeda disclose all limitations of claim 1. They do not disclose wherein each signal processing unit comprises a multiplexer at its input and

a demultiplexer at its output. However, the signal-processing unit comprising a multiplexer at its input and a demultiplexer at its output is a minor detail. Koseki et al. discloses in Fig. 4a, a signal-processing unit comprising a multiplexer (42) at its input and a demultiplexer (68) at its output. It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Koseki et al. as a method of permitting the simultaneous transmission of two or more trains of data over a single channel.

11. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda (US Patent 5,734,808) as applied to claims 2-3, respectively in view of Koseki et al. (US Patent 4,986,668).

As noted above, Takeda discloses all limitations of claims 2 and 3. Takeda does not disclose wherein each signal processing unit comprises a multiplexer at its input and a demultiplexer at its output. However, the signal-processing unit comprising a multiplexer at its input and a demultiplexer at its output is a minor detail. Koseki et al. discloses in Fig. 4a, a signal-processing unit comprising a multiplexer (42) at its input and a demultiplexer (68) at its output. It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Koseki et al. as a method of permitting the simultaneous transmission and reception of two or more trains of data over a single channel.

12. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda (US Patent 5,734,808) in view of Thomas et al. (US Patent 7,017,064 B2).

Takeda a transceiver unit adapted to communicate with a buffer unit via a bus system, the transceiver unit comprising, a transceiver controller (Fig. 15A, Out Put control, 220 controls transceiver of Fig. 1. Transceiver in the sense of receiving data and transmitting processed data) and a communication device (pipeline processing device of Fig. 1), both transceiver controller and communication device being interconnected, said communication device including a plurality of signal processing units (pipeline processing register, data processing) connected in sequence, each signal processing unit being clocked by a common clock signal (BCLK); and a control line (Pipeline Control) to which each signal processing unit is connected, the control line communicating flow control information either in the transmit mode to at least one of the preceding signal processing units or in the receive mode to at least one of the following signal processing units. (Takeda teaches a pipeline processing device wherein he teaches sequential transfer of data and communicating flow control information in a transmit mode to at least one of the preceding signal processing units (col. 2, lines 55-60; col. 3, lines 50-64; Takeda et al. teaches processing data transferred only when there is processing data in the previous stage).

Takeda does not explictly teach a mode line connected to each signal processing unit for switching each processing unit between a transmit mode and a receive mode.

However, Thomas et al. discloses bi-directional pipeline processors operating in a forward direction and then in a reverse direction. A mode line for switching each pipeline processors between a transmit/forward and receive/reverse mode of operation would be inherent.

One of ordinary skill in the art at the time of invention would have been motivated to incorporate the teachings of Thomas as a method of incorporating bi-directional processing in the system (col. 3, lines 32-52).

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 571-272-3037. The examiner can normally be reached on Monday-Friday (8:00-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ghayour Mohammad can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Tesfaldet Bocure/
Primary Examiner, Art Unit 2611

lbw
March 2, 2010